APPENDIX H

[~~Each~~] With reference to Figure 16, each semiconductor device contains a set of internal registers 170, preferably including a device identification (device ID) register 171, a device-type descriptor register 174, control registers 175 and other registers containing other information relevant to that type of device. In a preferred implementation, semiconductor devices connected to the bus contain registers 172 which specify the memory addresses contained within that device and access-time registers 173 which store a set of one or more delay times at which the device can or should be available to send or receive data.

Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset. During the initialization sequence each device on the bus is assigned a unique device ID number, which is stored in the device ID register 171. A bus master can then use these device ID numbers to access and set appropriate registers in other devices, including access-time registers 173, control registers 175, and memory registers 172, to configure the system. Each slave may have one or several access-time registers 173 (four in a preferred embodiment). In a preferred embodiment, one access-time register in each slave

is permanently or semi-permanently programmed with a fixed value to facilitate certain control functions. A preferred implementation of an initialization sequence is described below in more detail.